**Electrical Engineering**

**Subject: DIGITAL ELECTRONICS**

**(The answer keys are at the end.)**

1. An XOR (EX-OR) having two inputs the output exists (high) only when
2. Both inputs are high
3. Both inputs are low
4. When any one of the inputs is high and other is low
5. When a specified inputs is high or low
6. A NOR gate can function as
7. NOT gate only
8. OR gate only
9. AND gate only
10. All the above
11. The 1’s complement of 10101010 is
12. 01010101
13. 10101001
14. 00001111
15. 11110000
16. The logical expression is
17. A 32:1 MUX have \_\_\_\_\_\_ select lines
18. 3
19. 4
20. 5
21. 6
22. The number of NAND gates needed to construct a 2:4 line decoder is
23. 2
24. 4
25. 6
26. 8
27. A flip-flop can store \_\_\_\_ of information
28. 1 bit
29. 1 byte
30. 2 bit
31. 8 bit.
32. Latches are (1) storage devices (2) level sensitive devices
33. Only (1) is correct
34. Only (2) is correct
35. Both (1) and (2) are correct
36. Both (1) and (2) are incorrect
37. Figure-of-merit is basically the product of
38. Input and feedback signal
39. Speed and power
40. Voltage and current
41. Speed and input voltage
42. 64k byte is equivalent to \_\_\_\_\_byte
43. 221
44. 232
45. 216
46. 210
47. Which of the following digital logic circuits can be used to add more than 1 – bit simultaneously?
48. Full – adder
49. Ripple – carry adder
50. Half – adder
51. Serial adder
52. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop?
53. Two 2 input AND gates
54. Two 3 input AND gates
55. Two 2 input OR gates
56. Two 3 input OR gates
57. Race condition is
58. Always desirable feature of a digital circuit
59. Some times desirable in digital systems
60. Not desirable at all
61. Only dangerous if critical
62. The bit distance between all odd numbered columns in K-map is
63. Not fixed
64. Always 1
65. Always 2
66. Not specified.
67. can be simplified to
68. 1
69. B
70. 0
71. A NOR gate can be constructed from
72. NAND gate only
73. AND and NOT gate
74. OR gate and NOT gate
75. All the above
76. A simple flip-flop is a
77. 1 bit storage cell
78. 2 bit storage cell
79. 3 bit storage cell
80. 4 bit storage cell
81. In SR flip-flop, the conditions S=1 and R=0; S=0 and R=1 are known as respectively
82. Set and reset
83. Reset and set
84. Set and set
85. Reset and reset
86. In J-K flip-flop, if we input K with the inverted form of what we put J, the resulted flip flop is
87. SR flip-flop
88. JK flip flop
89. D flip flop
90. T flip flop
91. In a ring counter 1 for N clock pulses, the scale of the counter is
92. N:1
93. N:2
94. N:10
95. N:100
96. Which one of the following counter results in least decay
97. Ring counter
98. Ripple counter
99. Synchronous counter
100. Asynchronous counter
101. Which of the following is the fastest A/D converter?
102. Comparator converter
103. Counter type
104. Successive approximation
105. Dual slope type
106. In a 10-bit A/D converter, the quantization error is given by (in percent)
107. 1
108. 2
109. 0.1
110. 0.2
111. C
112. D
113. A
114. C
115. C
116. B
117. A
118. C
119. B
120. C
121. B
122. A
123. C
124. C
125. A
126. D
127. A
128. A
129. C
130. A
131. C
132. A
133. C